REMARKS

As a preliminary matter, Applicants thank the Examiner for the withdrawal of the previous claim objections and Section 112 rejections.

Claims 1-2, 4, 7, 9-10, 12, and 15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis (U.S. 6,321,298) in view of Kitamura et al. (U.S. 6,247,012). Applicants respectfully traverse this rejection for at least the reasons of record, and as follows. A *prima facie* case of obviousness has not been established. Neither of the cited references, whether taken alone or in combination, teaches or suggests that a first controller acquires a storage page in a mirror area of a second cache memory by referring to a first mirror management table in the first controller, as featured in independent claims 1 and 9 of the present invention, as last amended. Additionally, the Examiner has not pointed to any single teaching or suggestion from either reference that indicates the desirability of making the particular combination proposed by the Examiner.

The Examiner correctly recognizes, on page 6 of the outstanding Office Action, that Hubis fails to disclose mirror management tables that are included in controllers, as in the present invention. The Examiner relies only upon Kitamura for teaching such mirror management tables, and the Examiner further asserts that Kitamura teaches the relationship between the mirror management table of one controller with the second cache memory of the other controller. This assertion, however, is erroneous. Kitamura does not teach any such relationship between the mirror management table of one controller and the cache memory of the other.

In fact, the Examiner's remarks regarding the Kitamura reference appear to undermine the reliance on the reference. The Examiner asserts that Kitamura "discloses a mirror management table or managing a mirror area of a memory," but does not ever assert that Kitamura teaches or suggests any respective locations for the "mirror management table," the "mirror area," or the "memory." The failure to give consideration to these features of the present invention is highly significant, because the claimed interrelationship of these components is significant to the novelty of the invention.

For example, although the Examiner asserts that Fig. 12 of Kitamura discloses the mirror management table of the present invention, Fig. 12 shows only one single mirror management table 35 and one mirror control program 33 having a single mirror storage region 36. Fig. 12 of Kitamura does not teach or suggest any relationship between the mirror management table 35 and the cache or storage region of another controller. In fact, Kitamura teaches just the opposite. Kitamura specifically teaches that the mirror management table 35 relates to the mirror storage region 36 (col. 14, lines 28-39), both of which elements are clearly shown by Kitamura to connect to the *same* mirror control program (controller).

The rejection does refer to a "back-up copy of the primary data" and to a "secondary data storage system" from Kitamura, both of which the Examiner asserts to be taught at col. 2, lines 36-38. Applicants are at a loss though, to understand the Examiner's reference. Col. 2, lines 36-38 of Kitamura discusses only switching headlines of information displayed on one screen or another. The cited text portion does not refer to either of a "back-up copy of the primary data" or a "secondary data storage system." Fig. 12 of the reference

also fails to indicate any such elements. The rejection thus fails to cite to where the prior art teaches or suggests each and every claimed feature and limitation of the present invention, and therefore the outstanding rejection fails to establish a *prima facie* case of obviousness, as required by Section 2143.03 of the MPEP. Accordingly, the rejection should be withdrawn.

The rejection should also be withdrawn because it fails to indicate where, in either cited prior art reference, is a teaching or suggestion that supports the desirability of making the exact combination of references proposed by the Examiner. The Examiner appears to justify the proposed combination entirely on the assertion that the two references "are analogous art in that they both deal with managing the mirroring of data in distinct locations," and because Kitamura teaches, at col. 14, lines 21-25, only to use a mirror management tool with a system manager. Neither rationale, however, justifies the proposed combination under the requirements of Section 2143.01 of the MPEP.

Whether or not the two references are actually analogous art, as asserted by the Examiner, this fact alone, at most, would only suggest that the two references *can be* combined. Section 2143.01 though, expressly rejects such reasoning as being the basis for combining references. The mere fact that references can be combined does not establish the obviousness to make such a combination. Even if references can be combined, the Examiner still has the burden to establish where the art itself teaches or suggests the actual desirability of doing so.

The cited text from col. 14 of Kitamura fails to teach or suggest such desirability for the combination. The cited portion of Kitamura only suggests the benefits of

a mirror management tool that includes a table. As discussed above, Kitamura says nothing about the interaction of such a tool or table from one controller, with the specific cache memory in a second controller. Accordingly, even if a mirror table from Kitamura were added to the two controllers taught by Hubis, the Examiner has not cited to any teaching or suggestion from either reference that suggests how the management table of Kitamura would be incorporated into the dual controller system of Hubis in such a way that they would read upon the specific limitations recited in the present invention.

The Examiner asserts that the motivation for making the combination "would have been the ease of managing the storage locations in the memories mirror," but the Examiner does not indicate which memory he is referring to, and particularly with respect to the proposed combination of Kitamura with Hubis. Hubis discloses a significant number of different "memories," and the Examiner must be able to demonstrate that any proposed combination still reads upon all of the claimed limitations of the present invention, which has not been done in the present case. Accordingly, the asserted *prima facie* case of obviousness fails also under the requirements of Section 2143.01 of the MPEP, and it should be withdrawn for these reasons as well.

All of claims, 2, 4, 7, 10, 12, and 15 depend directly from one of independent claims 1 and 9, and therefore these dependent claims necessarily include all of the features of the respective base claim, plus additional features. Accordingly, Applicants respectfully traverse the rejection of these dependent claims for at least the reasons discussed above with respect to claims 1 and 9.

Claims 3 and 11 again stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis and Kitamura, and further in view of Tam et al. ("A Taxonomy-Based Comparison of Several Distributed Shared Memory Systems"). Applicants respectfully traverse this rejection for at least the reasons discussed above. Claims 3 and 11 depend from independent claims 1 and 9 respectively, and therefore also include all of the features of their respective base claim, plus additional features. Tam is cited merely for discussing the release of required pages, but not for any relationship between a mirror management table in a first controller, with the cache memory in a second controller.

Claims 5 and 13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis and Kitamura, in further view of Beardsley et al. (U.S. 6,304,980). Claims 5 and 13 indirectly depend from independent claims 1 and 9 respectively, and therefore should also be in condition for allowance for at least the reasons discussed above with respect to the independent claims. Beardsley is cited merely for its discussion of a controller disabling the processing to a mirror area of one cache memory, but not for anything relating to the relationship between a mirror management table in a first controller with the cache memory in the second controller.

Claims 6 and 14 again stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis and Kitamura, in further view of Rowson ("Interface-Based Design"). Applicants therefore respectfully traverse this rejection as well, for at least the reasons discussed above. Claims 6 and 14 depend from independent claims 1 and 9 respectively. Rowson is cited merely for its discussion of writing to more than one page, but

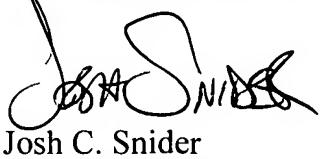
not for any teaching or suggestion relating to a relationship between the mirror management table of a first controller with the cache memory of a second controller.

Claims 8 and 16 again stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis and Kitamura, in further view of Li et al. ("Evaluation of Memory System Extensions"). Applicants respectfully traverse this rejection as well for at least the reasons discussed above. Claims 8 and 16 depend indirectly from independent claims 1 and 9 respectively. Li is cited merely for its discussion of DMA transfers, and not about the relationship between a mirror management table in a first controller with the cache memory from a second controller.

For all of the foregoing reasons, Applicants submit that this Application, including claims 1-16, is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 

Josh C. Snider
Registration No. 47,954

Customer No. 24978

November 21, 2006

300 South Wacker Drive
Suite 2500
Chicago, Illinois 60606
Telephone: (312) 360-0080
Facsimile: (312) 360-9315
P:\DOCS\3408\68745\AX5790.DOC